a first pixel value a first predetermined amount to form a first offset pixel value and . . . offsetting said first pixel value by the opposite of said first predetermined amount to form a second offset pixel value" as recited by Claim 1.

The Examiner has stated, "although Barbier et al does not teach the method of offsetting, but before performing the display, the adjacent pixel values have to offset inherently two different frames by the frame rate controlling of a graphic processor 2 (see figures 1, 3, 4, 12A and 12B, column 3, lines 34-50)."

The applicant respectfully submits that not only does Barbier fail to show, teach, or suggest the limitations of the independent claim, the Examiner has failed suggest how one of ordinary skill in the art would be led to construe the teachings of Barbier as teaching any sort of inherent offsetting as recited by Claim 1.

With respect to independent Claim 6, the Examiner has failed to provide a prima facie case of anticipation because the Examiner failed to provide any teaching in Barbier of "a logic circuit offsetting a first pixel value a first predetermined amount to form a first offset pixel value, said logic circuit also offsetting said first said pixel value by the opposite of said first predetermined amount to form a second offset pixel value; and display means displaying said first offset pixel value during a first display frame and displaying said second offset pixel value during a second display frame, such that the average of said displayed first offset pixel value and said second offset pixel value is said first pixel value" as recited by Claim 6.

The Examiner now states the recited logic circuit is taught by "a graphic processor 2 provides inherently a logic circuit offsetting a first bit a_{jk} stored in electrical form in a first memory plane A and a second bit b_{jk} stored in the second memory plane B (see figure 1, column 3, lines 11-16)."

The passage cited by the Examiner states, "The binary luminance of a pixel of the row L_j and the column C_k consists of the first bit a_{jk} stored in electrical form in a first memory plane A and a second bit b_{jk} stored in the second memory plane B. A sequencer circuit 7 produces the addressing of the memory 5 when reading and writing." The applicant submits the teachings of Barbier as repeated above simply do not support the Examiner's equating of Barbier's graphic processor to the recited logic circuit.

Claims 2-5 depend from Claim 1 and should be deemed allowable for that reason and on their own merits. Claims 7-10 depend from Claim 6 and should be deemed allowable for that reason and on their own merits.

In view of the remarks presented herewith, it is believed that the claims currently in the application, Claims 1-10, accord with the requirements of 35 U.S.C. § 112 and are allowable over the prior art of record. Therefore, it is urged that Claims 1-10 are in condition for allowance. Reconsideration of the present application is respectfully requested.

Respectfully submitted,

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